AK

Notice of Allowability	Application No.	Applicant(s)	
	10/796,823	TASI ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 07 November 2005*.

2. ☒ The allowed claim(s) is/are *2-8*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)
1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

BRADLEY K. SMITH
PRIMARY EXAMINER

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on November 7, 2005, which cancels claim 1 and presents claim 3 in independent form, has been entered.

Allowable Subject Matter

2. Claims 2-8 are allowed.

3. The following is an examiner's statement of reasons for allowance: a search of the relevant art did not find the method of forming an insulated isolation material layer on a V-shaped pit in an epitaxial layer and subsequently removing the isolation material from the surface of the epitaxial layer but leaving the isolation material in the V-shaped pit, as recited in claim 3.

Mishra et al. '144 discloses a method to reduce the dislocation density in group III-nitride films by growing a layer of group III-nitride on a substrate, passivating it with a silicon oxide layer, depositing an interlayer of InGaN, and continuing the group III-nitride layer growth process, however the silicon oxide is not on the surface of the III-nitride layer stack and the oxide is not removed from any parts of the III-nitride.

Kato et al. '192 and Ota et al. '839 disclose methods of making a group III-nitride device with lower dislocation density by forming a III-nitride film on a substrate, filling dislocations with AlGaN, and continuing to grow the III-nitride film, however an insulating isolation material is not used to passivate dislocations and the AlGaN barrier layer is not removed from portions of the III-nitride film.

Morita et al. '648 and Lee at el. '389 disclose methods to produce a crystalline film with low dislocation density formed by growing a monocrystalline layer on a substrate, etching the material to create pits along dislocations, filling the pits by coating the monocrystalline layer with silicon oxide or InGaN, and continuing to grow the monocrystalline layer. In both references, the pits are exacerbated by etching, and the silicon oxide barrier layer is not removed from any portion of the monocrystalline layer.

Watanabe et al. '846 discloses a method of manufacturing a nitride semiconductor device wherein a GaN film is formed on a substrate, and a second GaN layer is deposited on top of the first to fill in dislocations and prevent their further propagation. Hahn et al. '226 discloses a method of fabricating an LED comprising GaN layers, wherein the GaN layers have controlled thickness to control the development and propagation of dislocations. Neither reference discloses the use of an insulating barrier layer to passivate dislocations.

Nagai et al. '806 and Yang '823 disclose methods of manufacturing an LED comprising group III-V layers, wherein the final surface layer is passivated by a silicon oxide layer. Neither reference discloses removing portions of the silicon oxide from the surface and leaving portions in dislocation pits.

Nicolay et al. '207 discloses a method for fabricating isolated regions in a semiconductor device wherein V-shaped grooves are etched into the semiconductor surface, a field oxide is formed to fill the grooves, and the oxide is etched back to the semiconductor surface. This method is related to field oxide isolation and not to the passivation of group III-nitride dislocation pits.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sjf
11/21/05

BRADLEY K. SMITH
PRIMARY EXAMINER